

32768-word × 8-bit High Speed CMOS Static RAM

Features

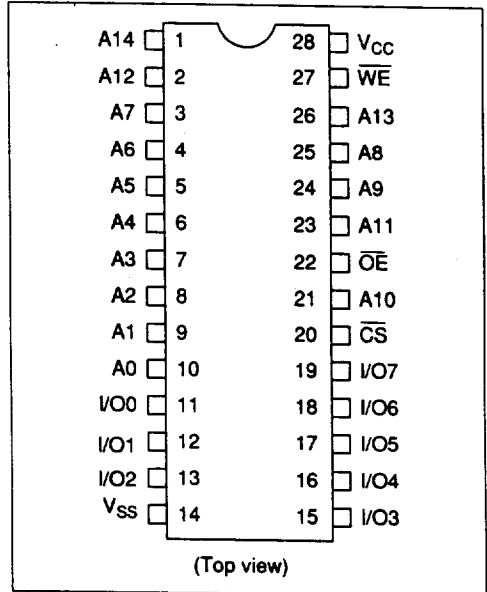
- High speed: Fast access time 85/100/120/150 ns (max)
- Low power standby and low power operation
 - Standby: 200 μ W (typ)/ 10 μ W (typ) (L-/L-SL-version)
 - Operation: 40 mW (typ) ($f = 1$ MHz)
- Single 5 V supply
- Completely static RAM: No clock or timing strobe required
- Equal access and cycle time
- Common data input and output, three-state output
- Directly TTL compatible—all inputs and outputs
- Battery back up operation capability (L-/L-SL-version)

Ordering Information

| Type No. | Access time | Package |
|----------------|-------------|----------------------------|
| HM62256P-8 | 85 ns | 600-mil 28-pin plastic DIP |
| HM62256P-10 | 100 ns | |
| HM62256P-12 | 120 ns | |
| HM62256P-15 | 150 ns | |
| HM62256LP-8 | 85 ns | |
| HM62256LP-10 | 100 ns | |
| HM62256LP-12 | 120 ns | |
| HM62256LP-15 | 150 ns | |
| HM62256LP-10SL | 100 ns | |
| HM62256LP-12SL | 120 ns | |
| HM62256LP-15SL | 150 ns | |

| Type No. | Access time | Package |
|------------------|-------------|--------------------|
| HM62256FP-8T | 85 ns | 28-pin plastic SOP |
| HM62256FP-10T | 100 ns | |
| HM62256FP-12T | 120 ns | |
| HM62256FP-15T | 150 ns | |
| HM62256LFP-8T | 85 ns | |
| HM62256LFP-10T | 100 ns | |
| HM62256LFP-12T | 120 ns | |
| HM62256LFP-15T | 150 ns | |
| HM62256LFP-10SLT | 100 ns | |
| HM62256LFP-12SLT | 120 ns | |
| HM62256LFP-15SLT | 150 ns | |

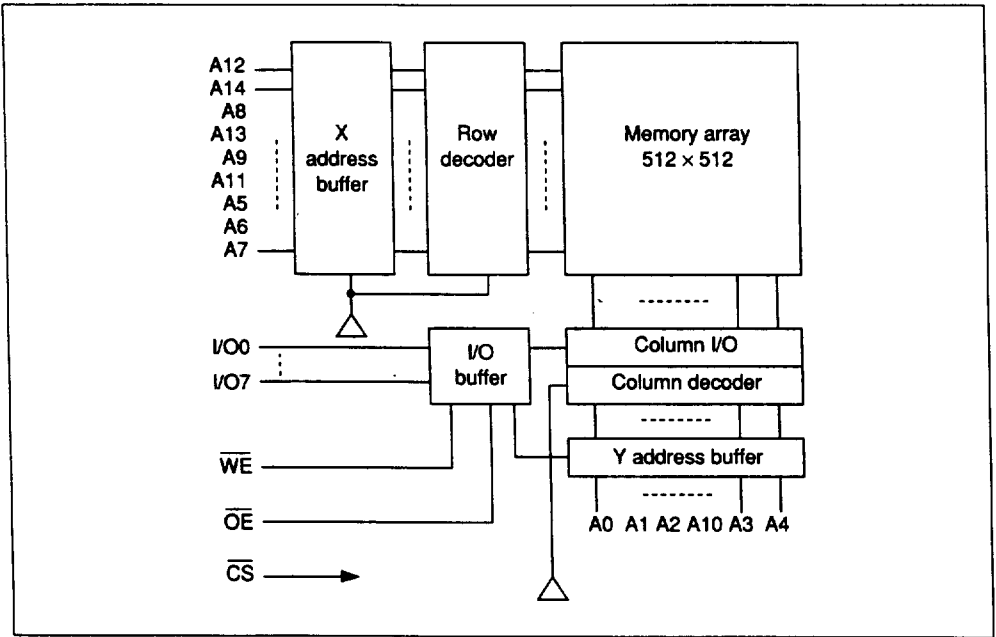
Pin Arrangement



Note: This device is not available for new application.

HM62256 Series

Block Diagram



Truth Table

| \overline{CS} | \overline{OE} | \overline{WE} | Mode | V_{CC} current | I/O pin | Reference cycle |
|-----------------|-----------------|-----------------|--------------|-------------------|---------|--------------------|
| H | x | x | Not selected | I_{SB}, I_{SB1} | High Z | — |
| L | L | H | Read | I_{CC} | Dout | Read cycle No. 1-3 |
| L | H | L | Write | I_{CC} | Din | Write cycle No. 1 |
| L | L | L | Write | I_{CC} | Din | Write cycle No. 2 |

Note: x means H or L

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|------------|---------------|------|
| Voltage on any pin relative to V_{SS} | V_T | -0.5* to +7.0 | V |
| Power dissipation | P_T | 1.0 | W |
| Operating temperature | T_{opr} | 0 to +70 | °C |
| Storage temperature | T_{stg} | -55 to +125 | °C |
| Temperature under bias | T_{bias} | -10 to +85 | °C |

Note: -3.0 V min for pulse width \leq 50 ns

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|----------|-------|-----|-----|------|
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input voltage | V_{IH} | 2.2 | — | 6.0 | V |
| | V_{IL} | -0.5* | — | 0.8 | V |

Note: -3.0 V min for pulse width \leq 50 ns

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0$ to +70°C)

| Parameter | Symbol | Min | Typ *1 | Max | Unit | Test condition | |
|--|------------|-----------|--------|-----|---------------|--|---|
| Input leakage current | $ I_{LI} $ | — | — | 2 | μA | $V_{IN} = V_{SS}$ to V_{CC} | |
| Output leakage current | $ I_{LO} $ | — | — | 2 | μA | $CS = V_{IH}$ or $OE = V_{IH}$ or $WE = V_{IL}$ $V_{IO} = V_{SS}$ to V_{CC} | |
| Operating power supply current | I_{CC} | — | 8 | 15 | mA | $CS = V_{IL}$, $I_{VO} = 0\text{ mA}$ | |
| Average operating power supply current | HM62256-8 | I_{CC1} | — | 50 | 70 | mA | Min. cycle, duty = 100%, $CS = V_{IL}$, $I_{VO} = 0\text{ mA}$ |
| | HM62256-10 | | — | 40 | 70 | mA | |
| | HM62256-12 | | — | 35 | 70 | mA | |
| | HM62256-15 | | — | 33 | 70 | mA | |
| | | I_{CC2} | — | 8 | 15 | mA | $CS = V_{IL}$, $V_{IH} = V_{CC}$, $V_{IL} = 0\text{V}$, $I_{VO} = 0\text{ mA}$, $f = 1\text{ MHz}$ |

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DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$) (cont)

| Parameter | Symbol | Min | Typ ¹ | Max | Unit | Test condition |
|------------------------------|-----------|-----|------------------|------------------|---------------|---|
| Standby power supply current | I_{SB} | — | 0.5 | 3 | mA | $\overline{CS} = V_{IH}$ |
| | I_{SB1} | — | 0.04 | 2 | mA | $\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $0\text{ V} \leq V_{IN}$ |
| | — | — | 2 ² | 100 ² | μA | — |
| | — | — | 2 ³ | 50 ³ | — | — |
| Output voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 2.1\text{ mA}$ |
| | V_{OH} | 2.4 | — | — | V | $I_{OH} = -1.0\text{ mA}$ |

- Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$ and specified loading.
2. These characteristics are guaranteed only for L-version.
3. These characteristics are guaranteed only for L-SL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Typ | Max | Unit | Test Condition |
|--------------------------|----------|-----|-----|------|-----------------------|
| Input capacitance | C_{IN} | — | 6 | pF | $V_{IN} = 0\text{ V}$ |
| Input/output capacitance | C_{VO} | — | 8 | pF | $V_{VO} = 0\text{ V}$ |

Note: These parameters are sampled and not 100% tested.

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }+70^\circ\text{C}$ unless otherwise noted)

AC Test Conditions:

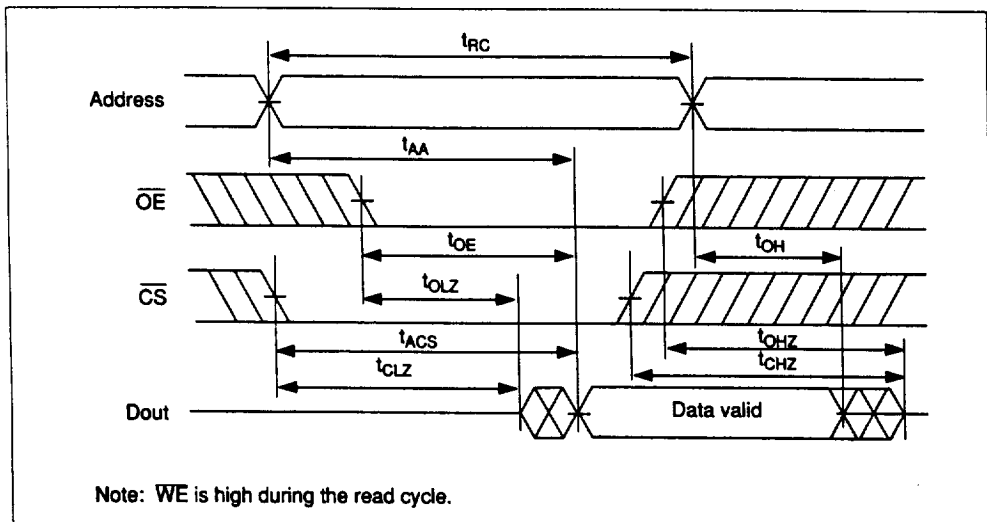
- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1TTL gate and $C_L = 100\text{ pF}$ (including scope and jig)

Read Cycle

HM62256-8 HM62256-10 HM62256-12 HM62256-15

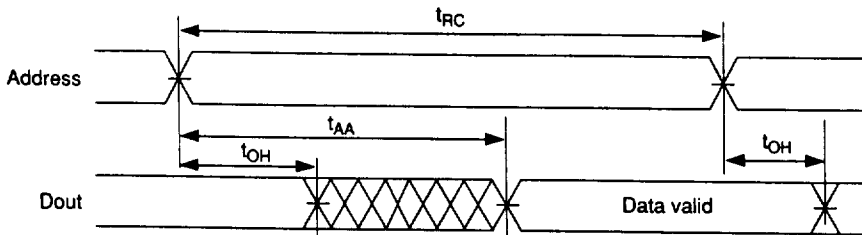
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | Unit |
|--------------------------------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| Read cycle time | t_{RC} | 85 | — | 100 | — | 120 | — | 150 | — | ns |
| Address access time | t_{AA} | — | 85 | — | 100 | — | 120 | — | 150 | ns |
| Chip select access time | t_{ACS} | — | 85 | — | 100 | — | 120 | — | 150 | ns |
| Output enable to output valid | t_{OE} | — | 45 | — | 50 | — | 60 | — | 70 | ns |
| Output hold from address change | t_{OH} | 5 | — | 10 | — | 10 | — | 10 | — | ns |
| Chip selection to output in low Z | t_{CLZ} | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| Output enable to output in low Z | t_{OLZ} | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| Chip deselection to output in high Z | t_{CHZ} | 0 | 30 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Output disable to output in high Z | t_{OHZ} | 0 | 30 | 0 | 35 | 0 | 40 | 0 | 50 | ns |

Read Timing Waveform (1)



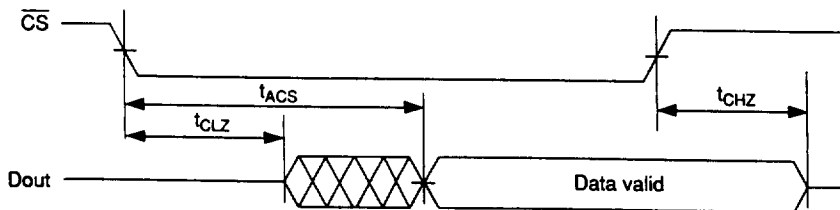
HM62256 Series

Read Timing Waveform (2)



- Notes:
1. \overline{WE} is high during the read cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. $OE = V_{IL}$.

Read Timing Waveform (3)

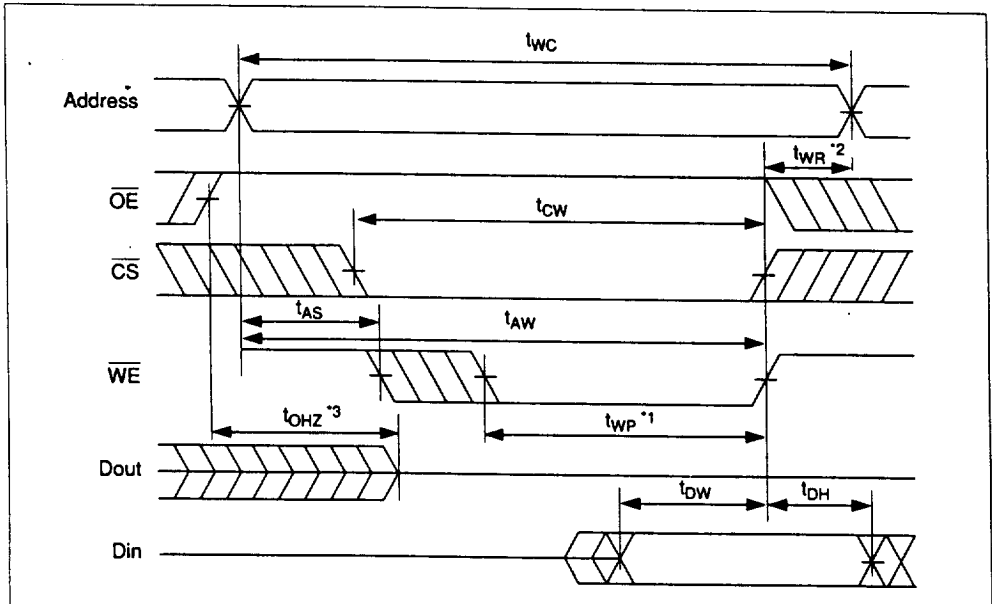


- Notes:
1. \overline{WE} is high during the read cycle.
 2. Address valid prior to or coincident with \overline{CS} transition low.
 3. $OE = V_{IL}$.

Write Cycle

| Parameter | Symbol | HM62256-8 | | HM62256-10 | | HM62256-12 | | HM62256-15 | | Unit |
|------------------------------------|-----------|-----------|-----|------------|-----|------------|-----|------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 85 | — | 100 | — | 120 | — | 150 | — | ns |
| Chip selection to end of write | t_{CW} | 75 | — | 80 | — | 85 | — | 100 | — | ns |
| Address valid to end of write | t_{AW} | 75 | — | 80 | — | 85 | — | 100 | — | ns |
| Address set up time | t_{AS} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Write pulse width | t_{WP} | 60 | — | 60 | — | 70 | — | 90 | — | ns |
| Write recovery time | t_{WR} | 10 | — | 0 | — | 0 | — | 0 | — | ns |
| Write to output in high Z | t_{WHZ} | 0 | 30 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Data to write time overlap | t_{DW} | 40 | — | 40 | — | 50 | — | 60 | — | ns |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Output disable to output in high Z | t_{OHZ} | 0 | 30 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| Output active from end of write | t_{OW} | 5 | — | 5 | — | 5 | — | 5 | — | ns |

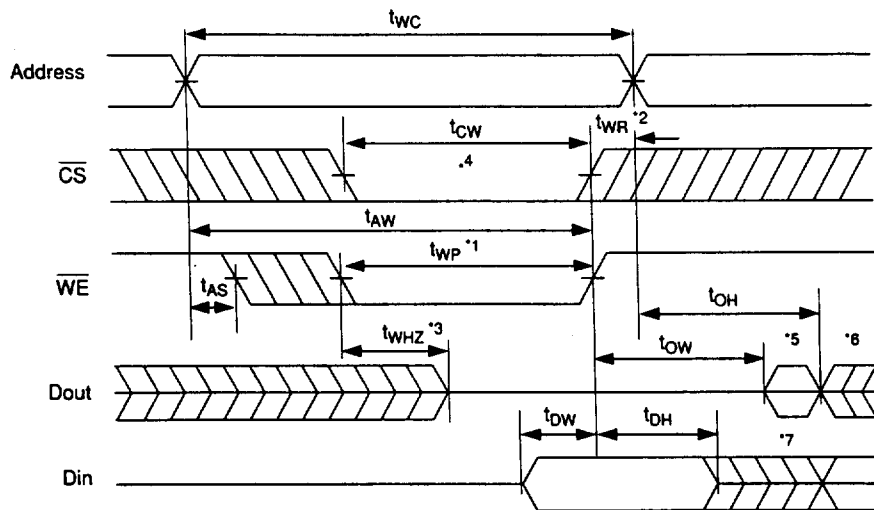
Write Timing Waveform (1) (\overline{OE} Clock)



- Notes:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state. Out of phase input signals must not be applied.

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Write Timing Waveform (2) (\overline{OE} Fixed Low)



- Notes:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} low transition, outputs remain in a high impedance state.
 5. Dout is in the same phase of written data of this write cycle.
 6. Dout is the read data of next address.
 7. If \overline{CS} is low during this period, I/O pins are in the output state. Out of phase input signals must not be applied to I/O pins.

Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

These characteristics are guaranteed only for L- and L-SL version.

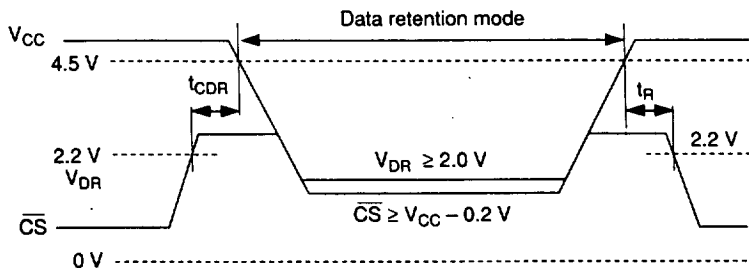
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------------|------------|--|---------------|-----|------------------------|---------------|
| V_{CC} for data retention | V_{DR} | $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ | 2.0 | — | — | V |
| Data retention current | I_{CCDR} | $V_{CC} = 3.0 \text{ V}$, $\overline{CS} \geq 2.8 \text{ V}$ $0 \text{ V} \leq V_{IN}$ | — | — | 50^{-2} 10^{-3} | μA |
| Chip deselect to data retention time | t_{CDR} | See retention waveform | 0 | — | — | ns |
| Operation recovery time | t_R | See retention waveform | t_{RC}^{*1} | — | — | ns |

Notes: 1. t_{RC} = read cycle time

2. These characteristics are guaranteed only for L-version, $V_{IL} = -0.3 \text{ V}$ min, $20 \mu\text{A}$ max. at $T_a = 0$ to 40°C .

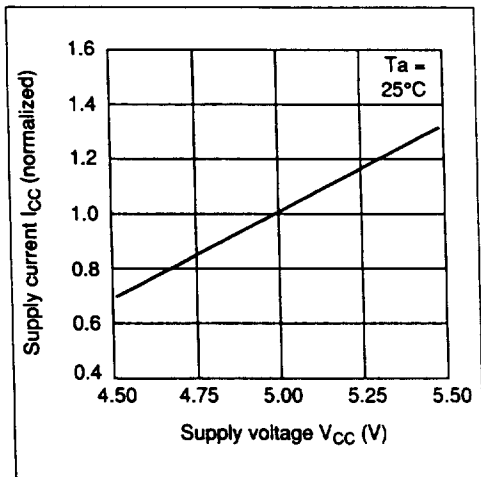
3. These characteristics are guaranteed only for L-SL version, $V_{IL} = -0.3 \text{ V}$ min, $3 \mu\text{A}$ max. at $T_a = 0$ to 40°C .

Low V_{CC} Data Retention Waveform

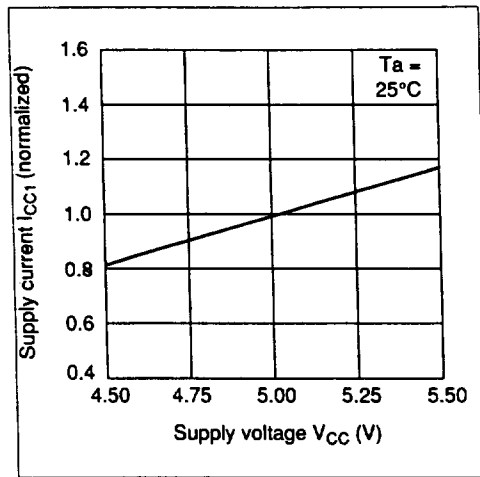


Note: In data retention mode, \overline{CS} controls the address, \overline{WE} , \overline{OE} , and D_{in} buffers. V_{in} for these inputs can be in high impedance state in data retention mode.

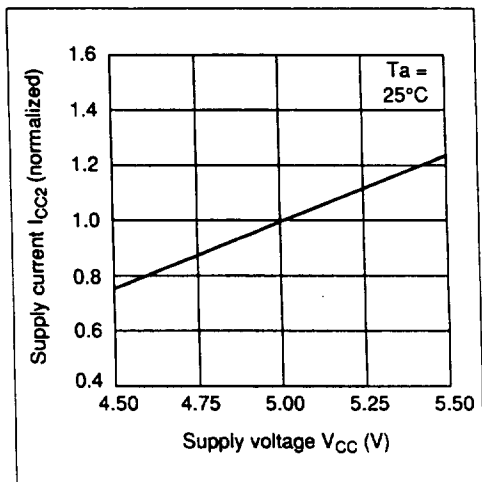
Characteristic Curves



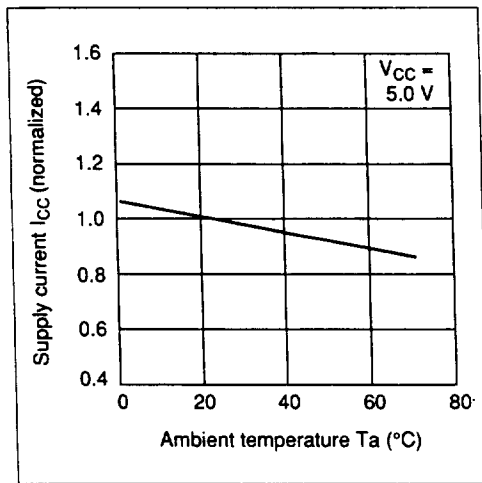
Supply Current vs. Supply Voltage (1)



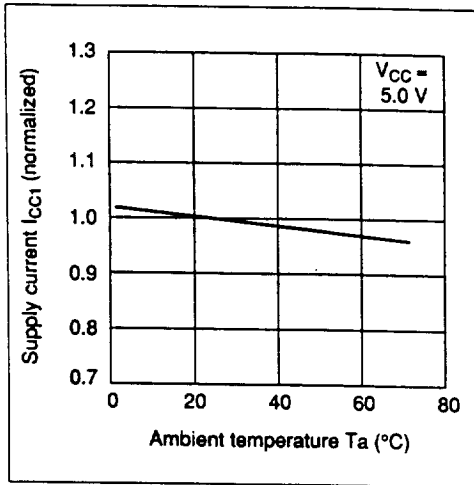
Supply Current vs. Supply Voltage (2)



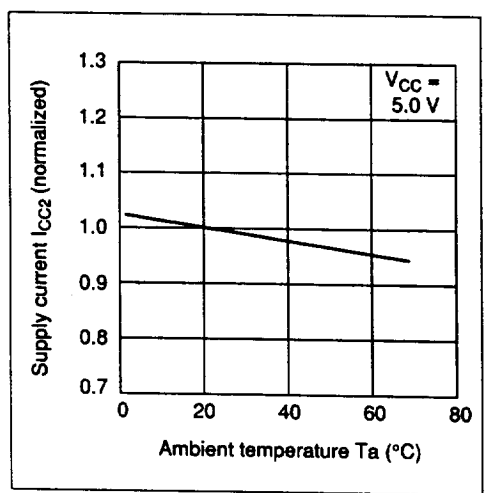
Supply Current vs. Supply Voltage (3)



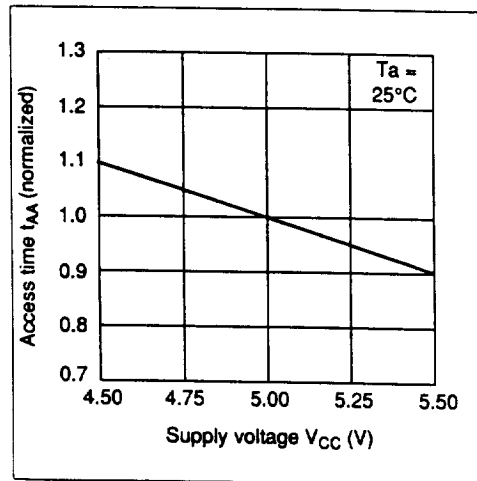
Supply Current vs. Ambient Temperature (1)



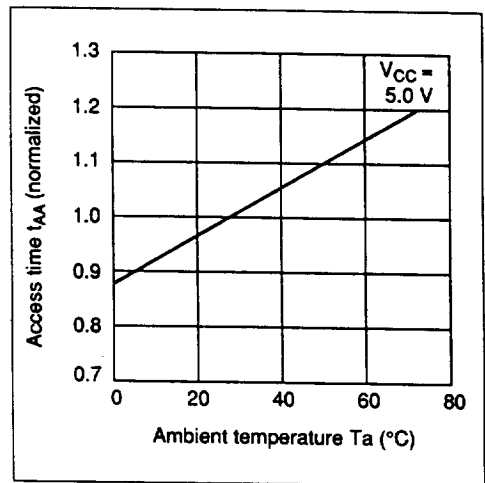
Supply Current vs. Ambient Temperature (2)



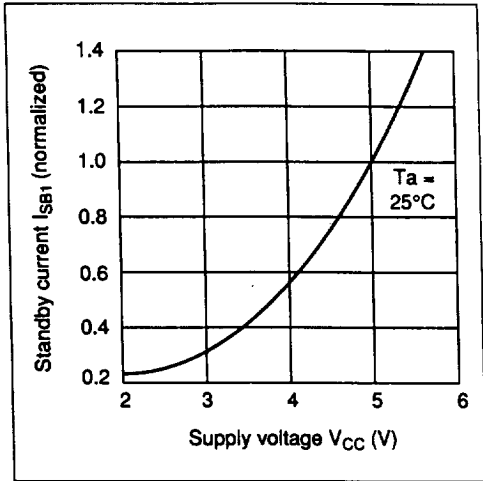
Supply Current vs. Ambient Temperature (3)



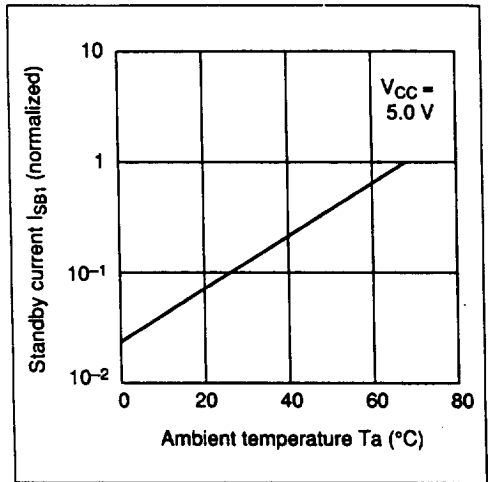
Access Time vs. Supply Voltage



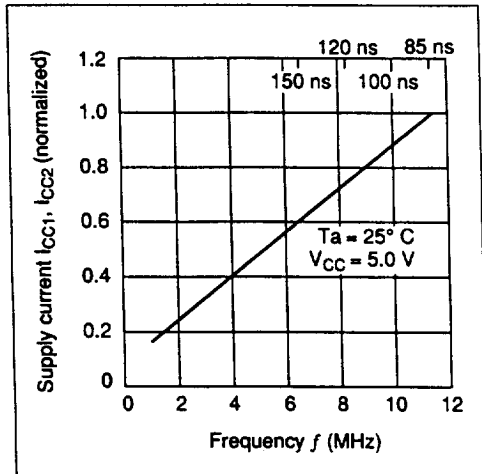
Access Time vs. Ambient Temperature



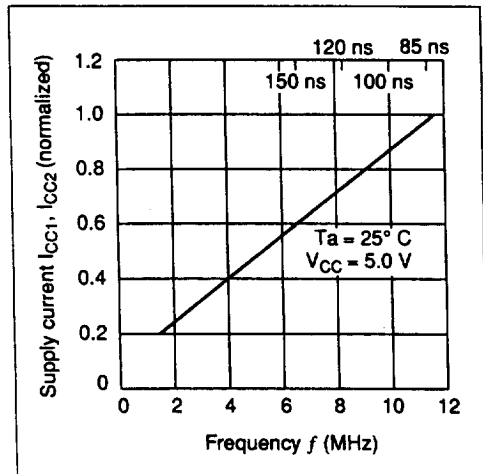
Standby Current vs. Supply Voltage



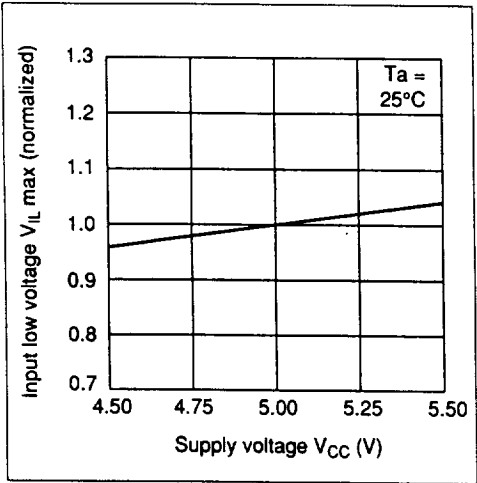
Standby Current vs. Ambient Temperature



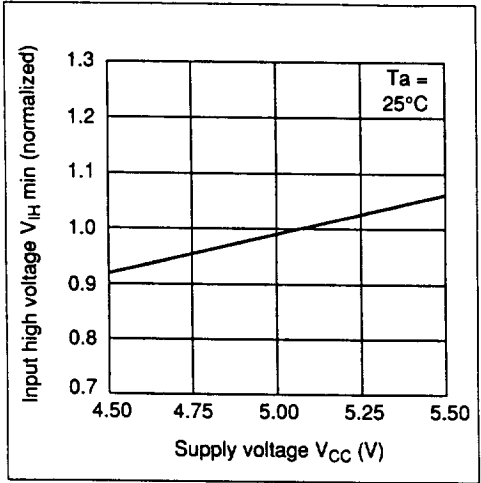
Supply Current vs. Frequency (Read)



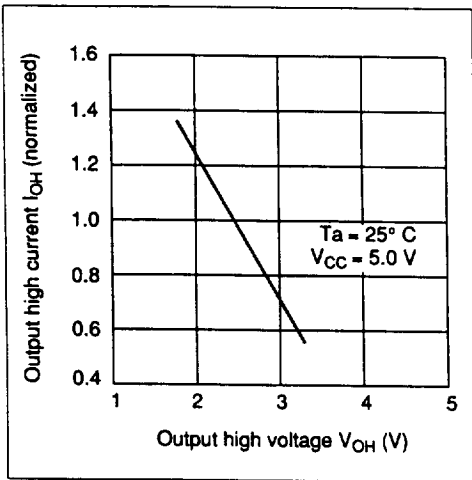
Supply Current vs. Frequency (Write)



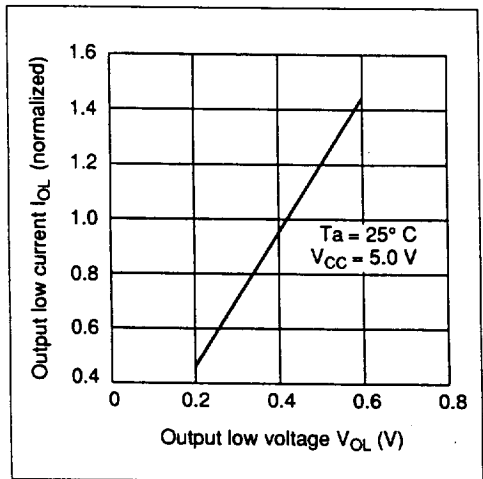
Input Low Voltage vs. Supply Voltage



Input High Voltage vs. Supply Voltage

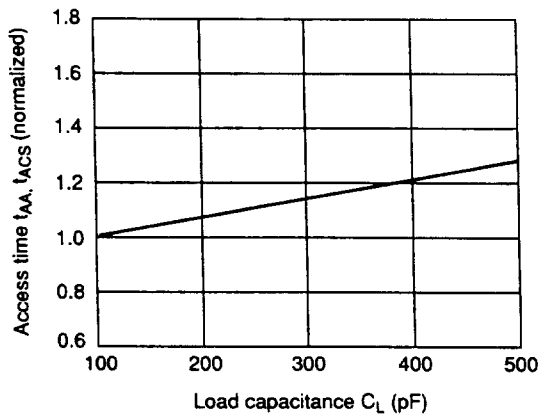


Output Current vs. Output Voltage (High)



Output Current vs. Output Voltage (Low)

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Access Time vs. Load Capacitance